

Chaitanya Prashanth

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EDUCATION

The George Washington University

Master of Science in Electrical and Electronics Engineering

GPA 3.96

Washington, DC

Jan. 2025 - May 2026

Relevant Courses: VLSI Design and Simulation, ASIC Design and Testing of VLSI circuits.

Dayananda Sagar College of engineering

Bachelor of Engineering in Electronics and Communication Engineering

GPA 3.66

Bengaluru, India

Aug. 2016 - Aug. 2020

Relevant Courses: Digital Signal Processing DSP, Logic Design, ARM, Microcontroller and Microprocessors

TECHNICAL SKILLS

Languages: Verilog, SystemVerilog, Python OOP, TCL, C, Bash

Tools: Cadence Virtuoso, Xcelium, Synopsys VCS, Vivado, Linux, Unix, Git, MATLAB, Jira, Perforce

Protocols: I2C, UART, SPI, USB, MIPI I3C, PCIe, AMBA, AXI/AHB/APB

Digital Concepts: SoC integration, DFT, CDC, RTL design microarchitecture and RTL coding, UVM

EXPERIENCE

ASIC Digital Design Engineer

July. 2022 - March. 2024

Synopsys, Inc.

Bengaluru, India

- Led Hardware FPGA Development prototyping and IP Validation in BareMetal and Linux platforms for I3C, an advancement of the I2C interface.
- Built end-to-end I3C IP microarchitecture hardware validation from circuit setup till SDK release, leveraging Synopsys ARC processor and HAPS FPGA platform, interfaced via AXI tunnel, JTAG, protocol analyzer, and Raspberry Pi. Configuration was modified to validate various features of the I3C IP.
- Validated IPs by simulation, debug simulation failures, synthesis, run regressions, Bitfile generation, packaging, register glue logic, C-tests, test planning and test reports, Compliance Testing with 99% feature coverage
- Coded constraint files for instrumented design, FPGA constraints, field constraints according to functional requirements and design specifications
- Debugged critical electrical ringing issue misinterpreted as In-Band Interrupts (IBI) from oscilloscope; resolved by optimizing trace lengths and component placement. Reducing signal feed-through issue by 42%.
- Increased data length of payload between I3C and target from 128bytes to 64kb by deploying High-Data-Rate (HDR) modes. Improved data transmission speed by 35%.
- Built FSM for vendor-specific I3C command handling and integrated it into full protocol stack, by collaborating with 4 member HW/SW team.
- Migrated prototyping platform from HAPS-DX7 to HAPS100 and upgraded the Regression Control Environment (RCE) delivering 4x faster performance and is crucial for I3C FPGA accelerator development, supporting speeds up to 12.5 MHz

Hardware Engineer

Oct. 2020 - July. 2022

L&T Technology Services Ltd

Bengaluru, India

- Conducted Board **Bring-up**, Circuit Board Layout in Altium ensuring IC power calculation, Signal Integrity and Power Integrity, AC timing analysis, Wire harness and Functional test for Texas Instruments (TI) sensors in hardware lab, ensuring 100% pass results. Here I used multimeters, power supplies and logic analyzer.

PROJECTS

Multi-Clock Domain SPI Memory Controller | Verilog RTL, Cadence Xcelium, Synopsys Design Compiler

Sep. 2025 - Nov. 2025

- Implemented SPI interface to read/write into a 256-address \times 16-bit register array with multicycle cross-domain crossing (CDC).
- Performed simulation, synthesis, and back-annotation, validating 1.8 ns propagation delays across 256 randomized read/write transactions. Achieved timing closure reporting positive slack (>6 ns) across clock domains.

Systolic Array for Matrix-Matrix Multiplication | Cadence Virtuoso, Spectre, ADE L

Oct. 2025 - Dec. 2025

- Designed weight-stationary systolic array integrating 4-bit multipliers, 11-bit carry-save adders, and registers to support pipelined multiply-accumulate (MAC) operations.
- Performed place and route, DRC, and LVS checks optimizing area through efficient adder design.
- Achieved 36% improvement in Energy-Delay Product (EDP) through PPA power, performance and area optimization.